

WHAT IS CLAIMED IS:

1. A multi-chip package comprising:

a circuit substrate consisting of first, second and
5 third areas which surround three sides of the multi-chip
package; and

at least two semiconductor chips which are positioned
within an internal space of the package defined by the
internal surfaces of the above three areas, wherein the
10 semiconductor chips are physically bonded and electrically
connected to each other.

2. The multi-chip package according to claim 1, wherein
the circuit substrate comprises a plurality of substrate
15 pads which are formed on the internal surfaces of the above
three areas and electrically connected to the semiconductor
chips.

3. The multi-chip package according to claim 1, wherein
20 the semiconductor chips comprises a plurality of chip pads
formed on the top surfaces of the semiconductor chips and a
plurality of chip bumps individually formed on each of the
chip pads, respectively corresponding chip bumps and
substrate pads being physically bonded and electrically

connected to each other.

4. The multi-chip package according to claim 1 or 3,
wherein the semiconductor chips comprises a first
5 semiconductor chip provided on the first area, at least one
second semiconductor chip provided on the second area, and a
third semiconductor chip provided on the third area.

5. The multi-chip package according to claim 4, wherein
10 a rear surface of the first semiconductor chip is faced to a
rear surface of the third semiconductor chip.

6. The multi-chip package according to claim 1, wherein
the first semiconductor chip and the third semiconductor
15 chip have an identical size.

7. The multi-chip package according to claim 2, wherein
the circuit substrate comprises a plurality of ball lands
which are formed on the external surface of the first area
20 and electrically connected to the substrate pads.

8. The multi-chip package according to claim 7, further
comprising a plurality of solder balls that are respectively
formed on the ball lands.

9. The multi-chip package according to claim 2, wherein the circuit substrate further comprises a fourth area that extends from a side of the third area.

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10. The multi-chip package according to claim 9, wherein the fourth area comprises a plurality of contact pads which are formed on a side of the fourth area and electrically connected to the substrate pads.

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11. The multi-chip package according to claim 1, wherein the circuit substrate comprises a plurality of notches being formed in the external surfaces of first, second and third areas at the boundaries of these three

15 areas.

12. The multi-chip package according to claim 1 or 11, further comprising an encapsulant filled in the internal space of the package.